PATENT
98095DIV4

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Gonzalez et al	:	
Group Art Unit:	:	SEMICONDUCTOR RAISED SOURCE-DRAIN STRUCTURE
Examiner:	:	
Serial No.	:	
Filed:	:	

PRELIMINARY AMENDMENT

November 9, 2001

Commissioner for Patents
Washington, DC 20231

Sir:

Prior to examination and prior to calculation of the application filing fee, please amend the above-identified application as follows:

In the Specification

Page 1, line 1, please insert:

- - CROSS REFERENCE TO RELATED APPLICATIONS

This is a divisional of copending United States patent application Serial No. 09/144,662, filed on September 1, 1998. - -

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Date of Deposit November 9, 2001

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Patricia A. Mack

In the Claims

Please cancel claims 1-16, 18, 20-28, and 31-97.

Please add the following new claims:

- - 98. The transistor of claim 17, wherein said raised source includes doped polysilicon.

99. The transistor of claim 17, wherein said raised drain includes doped polysilicon.

100. The transistor of claim 17, wherein said gate includes doped polysilicon.

101. The transistor of claim 17, wherein said source includes a plug.

102. The transistor of claim 101, wherein said plug includes an adhesive layer.

103. The transistor of claim 17, wherein said gate includes a gate terminal.

104. The transistor of claim 29, wherein said raised source includes doped polysilicon.

105. The transistor of claim 29, wherein said raised drain includes doped polysilicon.

106. The transistor of claim 29, wherein said gate includes doped polysilicon.

107. The transistor of claim 29, wherein said source includes a plug.

108. The transistor of claim 107, wherein said plug includes an adhesive layer.

109. The transistor of claim 29, wherein said gate includes a gate terminal.

110. The transistor of claim 29, wherein said first conductive path means includes a first junction.

111. The transistor of claim 110, wherein said first junction includes a doped silicon area.

112. The transistor of claim 111, wherein said doped silicon area includes phosphorous.

113. The transistor of claim 110, wherein said first junction extends beneath said gate, said source, and said drain.

114. The transistor of claim 110, wherein said first junction includes a pocket implant junction.

115. The transistor of claim 29, wherein said second conductive path means includes a second junction.

116. The transistor of claim 115, wherein said second junction includes a doped silicon area.

117. The transistor of claim 116, wherein said doped silicon area includes phosphorous.

118. The transistor of claim 115, wherein said second junction extends beneath said gate, said source, and said drain.

119. The transistor of claim 115, wherein said second junction includes a pocket implant junction.

120. The transistor of claim 29, wherein each of said first and second conductive path means includes a junction.

121. The transistor of claim 29, wherein each of said first and second conductive path means includes a junction.

122. The transistor of claim 29, wherein a portion of said raised drain is

substantially co-planar with a portion of at least one of said gate and said raised source.

123. The transistor of claim 29, wherein a portion of said gate is substantially co-planar with a portion of said raised source.

124. The transistor of claim 29, wherein a portion of said raised drain is substantially co-planar with at least a portion of both said gate and said raised source.

125. A transistor formed on a substrate assembly, comprising:

a gate structure;

a raised drain structure;

a raised source structure;

a first junction area in the substrate assembly between said gate structure and said raised drain structure, said first junction area extending beneath said gate structure and said raised drain structure; and

a second junction area in the substrate assembly between said gate structure and said raised source structure, said second junction extending beneath said gate structure and said raised source structure, wherein said first and second junction areas include doped silicon areas.

126. The transistor of claim 125, wherein said doped silicon areas include phosphorous.

127. A transistor formed on a substrate assembly, comprising:

a gate structure;

a raised drain structure;

a raised source structure;

a first junction area in the substrate assembly between said gate structure and said raised drain structure, said first junction area extending beneath said gate structure and said raised drain structure;

a second junction area in the substrate assembly between said gate structure and said raised source structure, said second junction extending beneath said gate structure and said raised source structure; and

wherein said first and said second junctions extend beneath said gate, said source, and said drain.

128. A transistor formed on a substrate assembly, comprising:

a gate structure;

a raised drain structure;

a raised source structure;

a first junction area in the substrate assembly between said gate structure and said raised drain structure, said first junction area extending beneath said gate structure and said raised drain structure;

a second junction area in the substrate assembly between said gate structure and said raised source structure, said second junction extending beneath said gate structure and said raised source structure; and

wherein said first and second junctions include pocket implant junctions. --

In the Drawings

Please substitute the enclosed set of five (5) sheets of formal drawings for those previously filed in United States patent application Serial No. 09/144,662, filed September 1, 1998 (herein the "parent application").

REMARKS

Applicants have amended the specification to indicate that the present application is a divisional of its parent application.

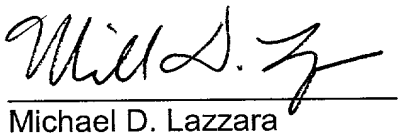
In addition, applicants have canceled claims 1-16, 18, 20-28, 31-97 to pursue non-elected claims 17, 19, 29 and 30 in the parent application. Furthermore, claims 98-128 have been added by the present amendment.

Enclosed is a set of five (5) sheets of formal drawings for filing with the present application. The drawings originally filed in the parent application should be replaced in the present application by this set of formal drawings.

SUMMARY

Entry of the present amendments and examination of the application at an early date are respectfully requested.

Respectfully submitted,



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